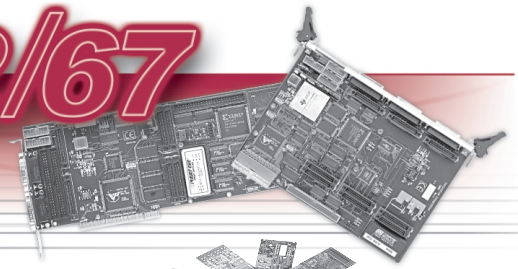
M62/67 cM62/67

Ultra-Performance DSP with Dual OMNIBUS I/O Sites



Features:

- TMX320C6201 DSP (fixed-point) or TMS320C6701 DSP (floating-point)
- Dual OMNIBUS Expansion Sites

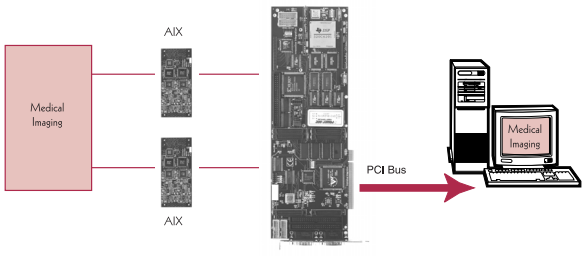
Applications:

- Video processing
- Adaptive control
- Multi-axis motion control
- Multichannel audio processing

Overview

Innovative Integration introduces a breakthrough in DSP technology. Based on Texas Instruments' revolutionary new TMS320C6x digital signal processors. With single-chip processing power in excess of 15 times that of any other single DSP, the 'C6x has redefined the DSP landscape and enabled access to an application performance plateau previously unreachable with anything but the largest of super-expensive massively-parallel computing systems.

Example Application



The 2.5 MHz input bandwidth and 16-bit resolution of the AIX module are ideal for many medical imaging applications. In this application, the M62/67 processes three-dimensional image data acquired from a patient scanning system prior to uploading via the PCI bus to a Windows application.

Processor Core

The M62/67 has a TMS320C6x 32-bit DSP as a data movement/data processing engine. On-chip peripherals include two 32-bit counter/timers, four powerful DMA channels, 1 Mbit on chip SRAM, a dedicated HPI parallel port interface and a prioritized interrupt controller. Memory on the M62/67 includes a 512 Kbyte asynchronous SRAM region (ASRAM) for bus mastering transfers and 16 Mbytes of 1 wait-state synchronous DRAM (SDRAM). Program memory may be expanded to include 1 Mbyte of 0 wait-state synchronous burst RAM (SBRAM).

On-board Peripherals

A simple, high-speed, memory-mapped, 32-bit latch is available to support general-purpose digital I/O. Direction is software-configurable in banks of eight bits. The port may be software or externally clocked at rates to 10 MHz.

The output of an AD9851 digital synthesizer is routed to each of two OMNIBUS sites, providing a time base spanning DC to 25 MHz programmable in increments of .02 Hz. Dedicated logic augments the on-chip timer and DDS complement to provide three additional 16-bit counter/timer channels which are often used as analog I/O and servo time bases. These timers may be internally or externally clocked but are normally clocked at 10 MHz.

Expansion

The M62/67 may be integrated with up to two OMNIBUS I/O module cards. Additionally, one 80 Mbyte/sec FIFO port is provided for high-speed digital communications and data acquisition applications.

The two OMNIBUS sites provide a flexible I/O expansion mechanism. Any in the ever-expanding suite of OMNIBUS modules may be used in any combination. Available modules include multichannel analog I/O at a variety of rates from DC to several MHz, digital I/O, RS232/422/485 serial communications, motion control and telephony. New modules are planned to facilitate very high-speed communications and RF down conversion. And since OMNIBUS is an elegant, open-architecture bus, custom modules may be designed easily and cost effectively to address unique application requirements.

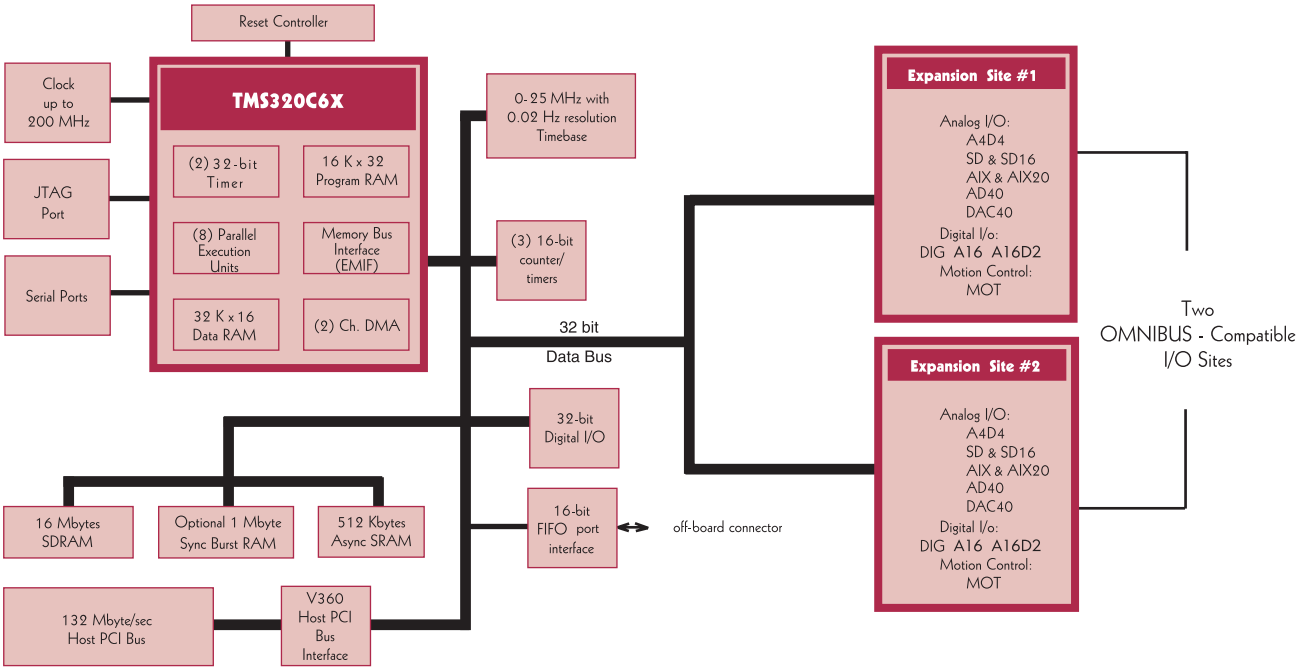
The M62/67's FIFOPort is useful to support dedicated board-to-board communications between multiple M62/67s or between the M62/67 and other Innovative 'C6x-based DSP boards, or with Chico

Host PC Interface

The M62/67 is a full-size card that plugs into a standard 32-bit PCI bus slot. ASRAM may be used for data storage and is the memory portal for PCI bus mastering transfers to and from the host PC. Data may be bus-mastered bidirectionally under the control of the 'C6x processor to the host PCs driver memory pool at sustained rates in excess of 30 Mbytes/sec. During bus master transfers, the M62/67 is free to perform data collection and analysis functions. Performance of such is unaffected by concurrent bus mastering operations unless the code accesses ASRAM, at which point bus arbitration may momentarily stall 'C6x global memory access. This global memory pool is also addressable as "dual-ported memory" to the host PC. Thus, applications may freely bus master or direct-address this memory for ultimate control and performance. Multiple cards may be installed in systems with full driver support under Windows 9x and NT.

OMNIBUS Modules Available

A4D1	Four A/D channels, 10 MHz/ch. w/14-bit resolution plus one 7.5 MHz D/A ch. 14-bit resolution
A4D4	Four A/D and four D/A channels at 200 kHz/channel with 16-bit resolution
A16D2	Sixteen A/D ch. at 200 kHz/ch. w/16-bit res. plus two D/A ch. at 200 kHz/ch. w/16-bit res.
AD16	Sixteen simultaneous channels, 16-bit, DC accurate, 195 kHz A/D
AD40	Two 40 MHz A/D channels at 12-bit resolution into 8-64K FIFOs
AIX	Four A/D channels at 2.5 MHz/channel with 16-bit resolution into an 8K FIFO
AIX20	Four A/D channels at 20 MHz/channel with 12-bit resolution into an 8K FIFO
DAC40	Four channel 14-bit 40 MHz D/A optimized for communications and telephony
DIG	32-bit digital I/O plus two async/sync serial ports
MOT	Four channel 16-bit 8 MHz for motion control
SD	Four A/D channels and four D/A channels at 96 kHz/channel with 100 dB S/N (24-bit)
SD16	Sixteen A/D channels and sixteen D/A channels at 48 kHz/channel with 18-bit resolution



Development Tools

The M62/67 is may be programmed in C or auto-optimized Assembler using the tools available in the Development Package. Components within this package fully support development of custom DSP applications. The Windows device driver and DLL provided in the toolset support host PC application development in Visual C or Basic, Borland C/Builder/Delphi and any other environment capable of linking to a standard Windows DLL or Active X control. Numerous target and host example programs are provided as well as support applets for terminal emulation, object file downloading, etc.

Alternately, the board is compatible with the new Ventura software library that provides full-bandwidth access to the peripheral complement of the M62/67 via a simple, elegant host API and packaged as a Windows DLL. Using Ventura, it is possible to exploit many of the vast data acquisition and processing capabilities of the M62/67 without writing any DSP code.

OEM Configurations

The M62/67 can be configured to fit your specific requirements and provide an optimal mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.

Software Options

Custom software for the M62/67 & cM62/67may be generated using the cross development tools.

Development Tools
TI C/Assembler
Code Hammer
Zuma Toolset

Ordering Information

M62

All M62 board configurations include: 160 MHz* TMS320C6201 processor; 0 Kbyte 0 wait-state program SBRAM; 16 Mbyte 1 wait-state SDRAM; 512 Kbyte 4 wait-state SRAM; two OMNIBUS I/O module sites; one high-speed FIFO port; two serial ports; 32-bit digital I/O; external multiplexer control; three 16-bit timers

Basic board
80012-0 Basic M62 board: 0 KB SBSRAM (Synchronous Burst SRAM)
Alternative cM62 board configurations
80012-2 M62 with 1024 KB 1 wait-state SBSRAM
Peripherals
80022-4 Screw-terminal breakout module and cable for 50-pin analog I/O connector
67013 High speed connectivity between FIFOPort compatible processor cards
Software and Support
53012 Zuma Toolset for M6x/cM6x
Hardware-assisted C/Assembler Source Level Debuggers
90021-5 Code Hammer with JTAG hardware/Code Composer software - for any 'C6x-based board
80021-2 Code Hammer with JTAG hardware only - for any TMS320 DSP-based board except 'C3x-based boards
54030 Code Composer software - for any 'C6x-based board
54037 Code Composer Studio- for any 'C6x-based board

Development Package
90012-0 Development Package for M62. Includes all of the following:

54015 Texas Instruments floating-point C compilation system for 'C6x
80012-0 Basic M62 board: 0 KB 0 wait-state SBSRAM (Synchronous Burst SRAM)
80022-4 Screw-terminal breakout module and cable for 50-pin I/O connector
51049 M62 hardware manual
51046 M62/cM62 software manual
52043 Texas Instruments TMS320C6x User's Guide
53012 Zuma Toolset for cM62
90021-5 Code Hammer with JTAG hardware/Code Composer software - for any 'C6x-based board

DevPack

M67

All M67 board configurations include: 150 MHz TMS320C6701 processor; 0 Kbyte 0 wait-state program SBRAM; 16 Mbyte 1 wait-state SDRAM; 512 Kbyte 4 wait-state SRAM; two OMNIBUS I/O module sites; one high-speed FIFO port; two serial ports; 32-bit digital I/O; external multiplexer control; three 16-bit timers

Basic board
80030-0 Basic M67 board: 0 KB SBSRAM (Synchronous Burst SRAM)
Alternative cM62 board configurations
80030-2 M67 with 1024 KB 1 wait-state SBSRAM
Peripherals
80022-4 Screw-terminal breakout module and cable for 50-pin analog I/O connector
67013 High speed connectivity between FIFOPort compatible processor cards
Software and Support
53009 Zuma Toolset for M67
Hardware-assisted C/Assembler Source Level Debuggers
90021-5 Code Hammer with JTAG hardware/Code Composer software - for any 'C6x-based board
80021-2 Code Hammer with JTAG hardware only - for any TMS320 DSP-based board except 'C3x-based boards
54030 Code Composer software - for any 'C6x-based board
54037 Code Composer Studio- for any 'C6x-based board

Development Package
90030-0 Development Package for M67. Includes all of the following:

54015 Texas Instruments floating-point C compilation system for 'C6x
80030-0 Basic M67 board: 0 KB 0 wait-state SBSRAM (Synchronous Burst SRAM)
80022-4 Screw-terminal breakout module and cable for 50-pin I/O connector
51049 M62/M67 hardware manual
51046 M62/M67 software manual
52043 Texas Instruments TMS320C6x User's Guide
53009 Zuma Toolset for M67
90021-5 Code Hammer with JTAG hardware/Code Composer software - for any 'C6x-based board

DevPack

cM62

All cM62 boards include: 160 MHz* TMS320C6201 processor; 0 KB 0 wait-state program SBRAM; 16 MB 1 wait-state SDRAM; 512 KB SRAM; three OMNIBUS I/O module sites; one high-speed FIFO port; two serial ports; 32-bit digital I/O; external multiplexer control; three 16-bit timers

Basic board
80015-0 Basic cM62 board: 0 KB SBSRAM (Synchronous Burst SRAM)
Alternative cM62 board configurations
80015-2 cM62 with 1024 KB 1 wait-state SBSRAM
Peripherals
80022-7 Screw-terminal breakout module and cable for 50-pin SCSI-2 analog I/O connector
67013 High speed connectivity between FIFOPort compatible processor cards
Software and Support
53012 Zuma Toolset for M62/cM62
Hardware-assisted C/Assembler Source Level Debuggers
90021-5 Code Hammer with JTAG hardware/Code Composer software - for 'C6x-based boards
80021-2 Code Hammer with JTAG hardware only - for TMS320 DSP-based boards except 'C3x-based boards
54030 Code Composer software - for any 'C6x-based board
54037 Code Composer Studio- for any 'C6x-based board

Development Package
90015-0 Development Package for cM62. Includes all of the following:

54015 Texas Instruments floating-point C compilation system for 'C6x
80015-0 Basic cM62 board: 0 KB 0 wait-state SBSRAM (Synchronous Burst SRAM)
80022-7 Screw-terminal breakout module and cable for 50-pin SCSI-2 analog I/O connector
51049 cM62 hardware manual
51046 M62/cM62 software manual
52043 Texas Instruments TMS320C6x User's Guide
53012 Zuma Toolset for cM62
90021-5 Code Hammer with JTAG hardware/Code Composer software - for any 'C6x-based board

DevPack

cM67

All cM67 boards include: 150 MHz* TMS320C6701 processor; 0 KB SBRAM; 16 MB 1 wait-state SDRAM; 512 KB SRAM; three OMNIBUS I/O module sites; one high-speed FIFO port; two serial ports; 32-bit digital I/O; external multiplexer control; three 16-bit timers

Basic board
80033-0 Basic cM67 board: 0 KB 0 wait-state SBSRAM (Synchronous Burst SRAM)
Alternative cM62 board configurations
80033-2 cM67 with 1024 KB 1 wait-state SBSRAM
Peripherals
80022-7 Screw-terminal breakout module and cable for 50-pin SCSI-2 analog I/O connector
67013 High speed connectivity between FIFOPort compatible processor cards
Software and Support
53009 Zuma Toolset for M67/cM67
Hardware-assisted C/Assembler Source Level Debuggers
90021-5 Code Hammer with JTAG hardware/Code Composer software - for 'C6x-based boards
80021-2 Code Hammer with JTAG hardware only - for any TMS320 DSP-based board except 'C3x-based boards
54030 Code Composer software - for any 'C6x-based board
54037 Code Composer Studio- for any 'C6x-based board

Development Package
90019-0 Development Package for cM67. Includes all of the following:

54015 Texas Instruments floating-point C compilation system for 'C6x
80033-0 Basic cM67 board: 0 KB SBSRAM (Synchronous Burst SRAM)
80022-7 Screw-terminal breakout module and cable for 50-pin SCSI-2 analog I/O connector
51049 cM67 hardware manual
51046 M67/cM67 software manual
52043 Texas Instruments TMS320C6x User's Guide
53009 Zuma Toolset for cM67
90021-5 Code Hammer with JTAG hardware/Code Composer software - for any 'C6x-based board

DevPack

* Contact Innovative Integration for availability of processor speeds.

For up to date pricing on all Innovative products visit www.innovative-dsp.com/webquote

Digital Signal Processor
Texas Instruments TMS320C6201 or TMS320C6701 DSP. On-chip resources: 64 K byte program/ 64 K byte data memory; two multichannel buffered serial ports; two 32-bit timers; four DMA channels; 32-bit external memory interface; DSP speed up to 200 MHz, depending on configuration

Memory Options
16 Mbytes synchronous DRAM (one wait-state)
1 Mbyte synchronous burst SRAM (zero wait-state)
512 K bytes asynchronous SRAM

Debug Port
JTAG 1149.1 compliant emulation port
Compatible with Innovative Code Hammer, TI XDS-510, or equivalent C/Assembler debugging using TI EVM or Code Composer software 2nd connector for easy JTAG chaining to other DSP cards

PCI Bus
32-bit PCI bus Advanced 2nd generation PCI bus controller. Master or slave interface; Bus Mastering interface, capable of 132 Mbytes/sec burst transfers; Typical performance 60 Mbytes/sec sustained under Win95/NT Plug-n-Play under Win95/NT

Digital I/O
32-bit programmable as input or output in groups of 8 TTL compatible with 32/-64 mA current capability Memory mapped FIFO Port 16-bit input and output Input data stream has 512 x 16 FIFO; 80 Mbytes/sec max data rate; memory-mapped

Timers/Counters
Two on-chip, 32-bit timers clocked at DSP speed / 4; three 16-bit, counter/timers clocked at 10 MHz or frequency synthesizer rate

Timebase
One programmable digital frequency synthesizer; 0-

Generation
25 MHz range in 0.02 Hz steps

OMNIBUS module Sites
Two expansion sites
Expansion using OMNIBUS modules for analog and digital I/O Compatible with all OMNIBUS modules 50 module-specific I/O connections per module

OMNIBUS the most I/O options available

A4D1	Four A/D channels, 10 MHz/ch. w/14-bit resolution plus one 7.5 MHz D/A ch. 14-bit resolution
A4D4	Four A/D and four D/A channels at 200 kHz/channel with 16-bit resolution
A16D2	Sixteen A/D ch. at 200 kHz/ch. w/16-bit res. plus two D/A ch. at 200 kHz/ch. w/16-bit res.
AD16	Sixteen simultaneous channels, 16-bit, DC accurate, 195 kHz A/D
AD40	Two 40 MHz A/D channels at 12-bit resolution into 8-64K FIFOs
AIX	Four A/D channels at 2.5 MHz/channel with 16-bit resolution into an 8K FIFO
AIX20	Four A/D channels at 20 MHz/channel with 12-bit resolution into an 8K FIFO
DAC40	Four channel 14-bit 40 MHz D/A optimized for communications and telephony
DIG	32-bit digital I/O plus two async/sync serial ports
MOT	Four channel 16-bit 8 MHz for motion control
SD	Four A/D channels and four D/A channels at 96 kHz/channel with 100 dB S/N (24-bit)
SD16	Sixteen A/D channels and sixteen D/A channels at 48 kHz/channel with 18-bit resolution

Operating Conditions & Physicals

Connectors
50-pin polarized male pin header for digital I/O
Two 14-pin polarized male pin headers for emulation
44-pin male header for FIFO Port
10-pin polarized male pin header for timers
Two 50-pin polarized male pin headers for I/O modules Two DB15 males for I/O modules
Two 10-pin male header pin headers for serial ports

Physical Description
Full-length PCI card ; conforms to PCI specification
Max component height 0.70 inches

Power Requirements
+5 V @ 1.2 A; +/-12 V (OMNIBUS module dependent)

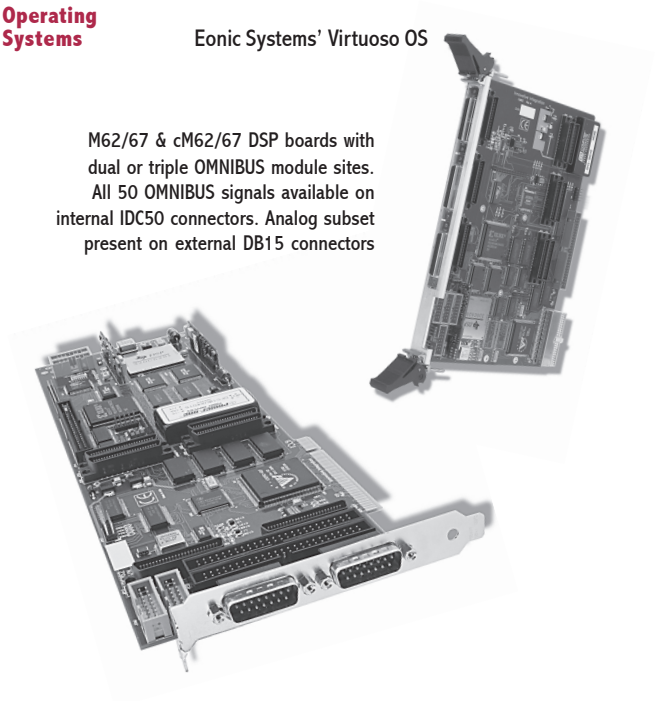
Operating Conditions
10-55 degrees C

Development Languages
C or Assembler using TI cross-development tools. Peripheral libraries and Windows drivers via Zuma Toolset

C/Assy Source Debugger
Code Hammer

Software Packages
Zuma Toolset, Ventura DLL, Code Composer Debugger

Operating Systems
Eonic Systems' Virtuoso OS



M62/67 & cM62/67 DSP boards with dual or triple OMNIBUS module sites. All 50 OMNIBUS signals available on internal IDC50 connectors. Analog subset present on external DB15 connectors